

PTO/SB/088 (08-03)

Approved for use through 07/31/2006. OMB 0651-0031

U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Substitute for form 1448/PTO

**INFORMATION DISCLOSURE
STATEMENT BY APPLICANT**

(Use as many sheets as necessary)

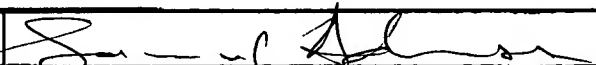
Complete if Known

Application Number	10/033,715
Filing Date	12/28/2001
First Named Inventor	Robert W. Bower
Art Unit	8633
Examiner Name	S. A. Gebremariam
Attorney Docket Number	BOW5075.04A

Sheet 1 of 1

NON PATENT LITERATURE DOCUMENTS

Examiner Initials ¹	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
8		Ellis, R. K. et al. "Electron Tunneling in Non-planar Floating Gate Memory Structure", IDEM, 1982, pp. 749-752.	
8		Shealy, J.R. et al. "Direct band gap structures on nanometer-scale, micromachined silicon tips", Appl. Phys. Lett. Vol. 70, No. 25, June 1997, pp. 3458-3460.	
8		Prickett, B.L. et al. "Trapping in Tunnel Oxides Grown on Textured Polysilicon", 21st annual Proceedings on Reliability Physics, 1983, pp. 114-117.	
8		Dimitrijević, S. "Understanding Semiconductor Devices", Oxford Press, New York, ISBN 019513186X, 2000, Chapter 8, Photonic Devices, Fig. 8.10.	
8		Neamen, D. "Semiconductor Physics & Devices - Basic Principles", second edition, ISBN 0256242143, 1997, p. 67.	
8		Mayer, J.W. "Electronic Materials Science: For Integrated Circuits in Si and GaAs", Macmillan Publishing, ISBN 0-02-378140-8, 1989, Section 14.8, pp. 431-436.	
8		Grove, A.S. "Physics and Technology of Semiconductor Devices", John Wiley and Sons, ISBN 0471329983, 1967, pp. 128-129.	
8		Sze, S.M. "Physics of Semiconductor Devices", Wiley-Interscience, ISBN 0471056618, 1981, pp. 46, 47, 690, 691.	
8		Wegener, H.A.R. et al. "The prediction of textured poly floating gate memory endurance", 23rd annual Proceedings on Reliability Physics, 1985, pp. 11-17.	

Examiner Signature		Date Considered	7/7/04
--------------------	---	-----------------	--------

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

1 Applicant's unique citation designation number (optional). 2 Applicant is to place a check mark here if English language Translation is attached. This collection of information is required by 37 CFR 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 2 hours to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

If you need assistance in completing the form, call 1-800-PTO-9199 (1-800-788-9199) and select option 2.